REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on <u>June 30, 2005</u>, and the references cited therewith.

Claims 1, 2, 5-7, 10, 13, 14, 17, 19, 23, 25, 26, and 28 are amended, and no claims are added or canceled; as a result, claims 1-28 are now pending in this application.

Information Disclosure Statement

Applicant respectfully requests that a copy of the 1449 Form, listing all references that were submitted with the Information Disclosure Statement filed on <u>November 5, 2003</u>, marked as being considered and initialed by the Examiner, be returned with the next official communication.

§112 Rejection of the Claims

Claims <u>5 and 6</u> were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 5 and 6 have been amended to recite "the method" rather than "the listed actions". Applicants believe that this rejection has been overcome by the amendment, and respectfully request that the rejection be withdrawn.

§102 Rejection of the Claims

Claims <u>1, 3-9, 11-19 and 21-28</u> were rejected under 35 USC § 102(b) as being anticipated by <u>Terauchi</u> (U.S. Patent No. 5,862,147). Terauchi discloses a method to perform wafer level tests of circuits. (See column 3, line 60 to column 4 line 1 of Terauchi). As described in Terauchi, an external tester supplies a test control signal on wiring 32*f* in parallel to pads 31*f* of all semiconductor devices 10 on the wafer 11. Applicant respectfully submits that the Terauchi reference does not disclose any method or apparatus that supports performing blank checks when a memory device is in use in a system. For example, the circuits of Terauchi do not support the blank checking of a FLASH memory device by a processor that is external to the FLASH memory device. The independent claims in the instant application have been amended to make

this distinction, and Applicant respectfully believes that the claims as amended clearly define over Terauchi.

Regarding independent claim 1, limitations have been added to make clear the distinction over Terauchi. For example, Terauchi does not disclose, teach, or suggest programming a FLASH memory device by issuing commands to a command register within the FLASH memory device, reading a status bit in a status register within the FLASH memory device, and programming the FLASH memory device. Applicant notes that the method of claim 1 is a method performed by a device outside the FLASH memory device. For example, the method of claim 1 may be performed by a device programmer such as device programmer 410 (Figure 4), or a processor such as processor 510 (Figure 5). This is in contrast to the method described in Terauchi, where a controller co-located with the memory performs operations in response to stimuli from an external tester.

Regarding independent claim 7, limitations have been added to make clear the distinction over Terauchi. For example, Terauchi does not disclose, teach, or suggest blank checking and programming a FLASH memory by receiving a blank check command from a device external to the FLASH memory device, reading a plurality of memory locations, and writing to a bit in a status register that is accessible by the device external to the FLASH memory. Applicant notes that the method of claim 7 is a method performed by a FLASH memory device when communicating with a device external to the FLASH memory device. This is in contrast to the method described in Terauchi, where a controller co-located with the memory performs operations in response to stimuli from an external tester.

Regarding independent claim 13, limitations have been added to make clear the distinction over Terauchi. For example, Terauchi does not disclose, teach, or suggest a memory device having a FLASH memory core, a control block, and an external interface to allow communication between the control block and a device external to the memory device, wherein the control block is capable of blank checking the at least a portion of the FLASH memory core during a programming operation when the memory device is in use in a system. In contrast, the controller of Terauchi is only described as performing operations during a wafer level test.

Independent claims 19 and 26 have been amended in a manner similar to claim 1, and are believed to define over Terauchi as a result. Further, independent claim 23 has been amended in a manner similar to claim 13, and is believed to define over Terauchi as a result.

Accordingly, independent claims 1, 7, 13, 19, 23, and 26 are believed to be in condition for allowance. Additionally, the dependent claims rejected as being anticipated by Terauchi all depend on the independent claims described above, and are believed to be in condition for allowance at least by virtue of dependency.

§103 Rejection of the Claims

Claims 2, 10 and 20 were rejected under 35 USC § 103(a) as being unpatentable over Terauchi (U.S. Patent No. 5,862,147) in view of Salzman (U.S. Patent No. 5,438,536). This rejection relies on the anticipation of the independent claims upon which claims 2, 10, and 20 depend. As described above, applicant believes that the rejection of the independent claims has been overcome by amendment and remarks. Accordingly, applicant also believes that this rejection has been overcome by the same amendments and remarks.

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Title: FLASH MEMORY BLANK CHECK
Assignee: Intel Corporation

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (952-473-8800) to facilitate prosecution of this application.

Respectfully submitted,

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By his Representatives,

Customer Number 45445
Telephone Number 952-473-8800

Date   *9-20-05*   By   _____
                       Dana B. LeMoine
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this _20_ day of September, 2005.

_____   _____

Name   Signature